AMENDMENTS

In The Claims:

1. (Currently amended) A method of buffer management and task scheduling for two-dimensional data transforming, comprising the steps of:

(a) reading out old data in a block-by-block pattern and immediately writing in new data in a line-by-line pattern using a first mapping scheme; and

(b) reading out a following old data in a block-by-block pattern and immediately writing in a following new data in a line-by-line pattern using a second mapping scheme,

wherein the first mapping scheme and the second mapping scheme are interleaved in use, and satisfying requirement of a data sequence of the two-dimensional data transforming.

2. (Original) The method of claim 1, wherein an initialization step prior to step (a) is performed so as to set up a write logic address and a read logic address to zero.

3. (Original) The method of claim 2, wherein the write logic address is incremented by 1 per write and the read logic address is incremented by I per read.

4. (Original) The method of claim 1, wherein the data transforming is a two-dimensional Discrete Cosine Transform.

5. (Original) The method of claim 1, wherein the first and second mapping scheme translate logical addresses to physical addresses.

6. (currently amended) A method of buffer management and task scheduling for two-dimensional data transforming, which transforms data in a buffer sequentially by blocks, wherein a block comprises a specific size having plurality of row portions and a plurality of column portions, comprising the steps of:

(a) reading out old data in a block-by-block pattern and immediately writing in new data in a line-by-line pattern in the block using a first mapping scheme;

(b) moving the block to transform another column portion; and

(c) reading out old data in a block-by-block pattern and immediately writing in new data in a line-by-line pattern in the block using a second mapping scheme,

wherein the first mapping scheme and the second mapping scheme are interleaved in use, and satisfying requirement of data sequence of the two-dimensional data transforming.

7. (Original) The method of claim 6, wherein an initialization step prior to step (a) is performed so as to set up a write logic address and a read logic address to zero.

8. (Original) The method of claim 7, wherein the initialization step comprises completely filling the block with data using the second mapping scheme.

9. (Original) The method of claim 8, wherein the write logic address is incremented by 1 per buffer write and the read logic address is incremented by 1 per buffer read.

10. (Currently amended) The method of claim 6, [~~wherein~~] after the step (c) further comprising step (d) [~~comprises~~] moving the block to transform another column portion.

11. (Original) The method of claim 10, wherein step (a) to step (d) are repeated until the whole data in the buffer is transformed.

12. (Original) The method of claim 6, wherein the data transforming is a two-dimensional Discrete Cosine Transform.

13. (Original) The method of claim 6, wherein the buffer is a pre-buffer.

14. (Original) The method of claim 6, wherein the buffer is a staging buffer.

15. (Original) The method of claim 6, wherein the block has an 8x8 block size.

16. (Original) The method of claim 6, wherein the data is an image comprising 512 pixels of columns and 8 lines of rows.

17. (Original) The method of claim 16, wherein each pixel has a 9-bit pixel address which is separated to a 3-bit dot address, 3-bit block address and a 3-bit sector address and wherein each line is a 3-bit line address.

18. (Original) The method of claim 6, wherein the first and second mapping scheme translate logical addresses to physical addresses.

19. (Original) The method of claim 18, wherein the physical address in the first mapping scheme is equivalent to {sector address, line address, block address, dot address}.

20. (Original) The method of claim 18, wherein the physical address in the second mapping scheme is equivalent to {sector address, block address, line address, dot address}.

21. (currently amended) A method of buffer management and task scheduling for two-dimensional data transforming, which transforms data in a buffer sequentially by blocks, wherein a block comprises a specific size having plurality of row portions and a plurality of column portions, comprising the steps of:

(a) initializing a write logic address and a read logic address to zero;

(b) reading out old data in a block-by-block pattern and immediately writing in new data in a line-by-line pattern in the block using a first mapping scheme, wherein the write logic address and the read logic address is incremented by 1;

(c) moving the block to transform another column portion; and

(d) reading out old data in a block-by-block pattern and immediately writing in new data in a line-by-line pattern in the block using a second mapping scheme, wherein the write logic address and the read logic address is incremented by 1,

wherein the first mapping scheme and the second mapping scheme are interleaved in use, and satisfying requirement of a data sequence of the two-dimensional data transforming.

22. (Original) The method of claim 21, wherein the step (a) comprises completely filling the block with data using the second mapping scheme and incrementing the write logic address by 1.

23. (Currently Amended) The method of claim 21, [~~wherein~~] after step (d) further comprising step (e) [~~comprises~~] moving the block to transform another column portion.

24. (Original) The method of claim 23, wherein step (b) to step (e) are repeated until the whole data in the buffer is transformed.

25. (Original) The method of claim 21, wherein the data transforming is a two-dimensional Discrete Cosine Transform.

26. (Original) The method of claim 21, wherein the buffer is a pre-buffer.

27. (Original) The method of claim 21, wherein the buffer is a staging buffer.

28. (Original) The method of claim 21, wherein the block has an 8x8 block size.

29. (Original) The method of claim 21, wherein the data is an image comprising 512 pixels of columns and 8 lines of rows.

30. (Original) The method of claim 29, wherein each pixel has a 9-bit pixel address which is separated to a 3-bit dot address, 3-bit block address and a 3-bit sector address and wherein each line is a 3-bit line address.

31. (Original) The method of claim 21, wherein the first and second mapping scheme translate logical addresses to physical addresses.

32. (Original) The method of claim 31, wherein the physical address in the first mapping scheme is equivalent to {sector address, line address, block address, dot address}.

33. (Original) The method of claim 31, wherein the physical address in the second mapping scheme is equivalent to {sector address, block address, line address, dot address}.